MT6176 RF System Datasheet

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Document Revision History

Revision	Date	Author	Description
0.8	2015-05-08	CS Chiu Amos Wu Dimitris Nalbantis Hsinhung Chen Mike Durrant Chiyao Yu SC Yen YT Lu Yen-Tso Chen Li-Han Hung	Initial version
0.9	2015-06-09	Nomo Chen	Update BSI read protocol. Section 8.3
1.0	2015-07-23	Mike Durrant	Revised TX Pmax definitions & powers
1.1	2015-10-23	Amos Wu	1. Add section 3.2 2. Modify the table of contents
1.2	2016-03-18	Mike D	Added TX table 6.3 for CCA Cat 7.
1.3	2016-05-13	Yen-Tso Chen	Added section 5.3 for 26MHz clock buffer output
1.4	2016-12-9	Amos Wu	1. Update POD illustration in sec. 3.1 2. Correct the typo in the revision number
1.5	2017-2-17	Amos Wu	1. Update section 1.2, add B66 2. Update section 3.6, operating temperature
1.6	2017-03-08	Amos Wu	1. Add section 3.8
1.7	2017-04-12	Amos Wu	1. Remove table 6-1 for consistence
1.8	2017-04-13	Yen-Tso Chen	1. Update table 5-3

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1 Introduction

1.1 Overview

MT6176 is a multi-mode multi-band highly integrated transceiver in 40nm CMOS. This document describes the performance targets for the RF stand-alone chip to be embedded in the overall platform.

1.2 Key Features

- Full multi-mode RF solution (C2K/GGE/WCDMA/TDSCDMA/LTE/LTE-CA)
  - Multi-band LTE/WCDMA/TD-SCDMA/GGE/C2K

3GPP band			GGE	UMTS	TD-SCDMA	LTE FDD	LTE TDD	CDMA2000	3GPP2 band		
FDD	DL low	DL high							FDD	DL low	DL high
1	2110 MHz	2170 MHz		●		●		●	BC6	2110MHz	2170MHz
2	1930 MHz	1990 MHz	●	●		●		●	BC1	1930MHz	1990MHz
3	1805 MHz	1880 MHz	●	●		●					
4	2110 MHz	2155 MHz		●		●		●	BC15	2110MHz	2155MHz
5	869 MHz	894MHz	●	●		●					
6	875 MHz	885 MHz		●		●					
7	2620 MHz	2690 MHz				●					
8	925 MHz	960 MHz	●	●		●					
9	1844.9 MHz	1879.9 MHz		●		●					
10	2110 MHz	2170 MHz				●					
11	1475.9 MHz	1495.9 MHz		●		●					
12	729 MHz	746 MHz				●					
13	746 MHz	756 MHz				●					
14	758 MHz	768 MHz				●					
17	734 MHz	746 MHz				●					
18	860 MHz	875 MHz		●		●					
19	875 MHz	890 MHz		●		●					
20	791 MHz	821 MHz				●					
21	1495.9 MHz	1510.9 MHz				●					
22	3510 MHz	3590 MHz									
23	2180 MHz	2200 MHz				●					
24	1525 MHz	1559 MHz				●					
25	1930 MHz	1995 MHz				●					
26	859 MHz	894 MHz				●		●	BC0	860MHz	894MHz
27	852 MHz	869 MHz				●					
28	758 MHz	803 MHz				●					
29	717 MHz	728 MHz				●					
30 (WCS)	2350 MHz	2360 MHz				●					
66	2110 MHz	2200 MHz				●					
								●	BC4	1840MHz	1870MHz
								●	BC10	851MHz	940MHz
TDD	DL low	DL high									
33	1900 MHz	1920 MHz					●				
34	2010 MHz	2025 MHz			●		●				
35	1850 MHz	1910 MHz					●				
36	1930 MHz	1990 MHz					●				
37	1910 MHz	1930 MHz					●				
38	2570 MHz	2620 MHz					●				
39	1880 MHz	1920 MHz			●		●				
40	2300 MHz	2400 MHz			●		●				
41	2496 MHz	2690 MHz					●				
44	703 MHz	803 MHz					●				

  - 16QAM UL/64QAM DL (HSPA+/LTE)
  - C2K/2G/3G/4G co-banding
  - Supports RxD (14 RxD ports)
  - Supports SRLTE
- Direct Conversion (LTE/3G/8-PSK) and DFM for GMSK
  - Dedicated power detection circuits for power control over specific power range
  - 4LB/4MB/2HB TX output port

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- Hybrid Direct-Conversion (4G/3G/C2K)/Low-IF (GGE, DC-HSDPA) receiver
    - 14+14 RX input ports
    - 4 RXIF IQ outputs
- Low supply current & operation directly from dual DC-DC converters
- 26MHz from external VCTCXO operation (with integrated AFC DAC)
- Support RF Calibration features for key Rx and Tx specifications (Image rejection, LO feedthrough, IIP2, DC offset, RC corner)
- Temperature Measurement sub-system
- Carrier aggregation (CA)
    - All intra-band and inter-band CA combinations defined in 3GPP R12 (V12.6.0) are supported

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2 Block Diagram and Application Diagram

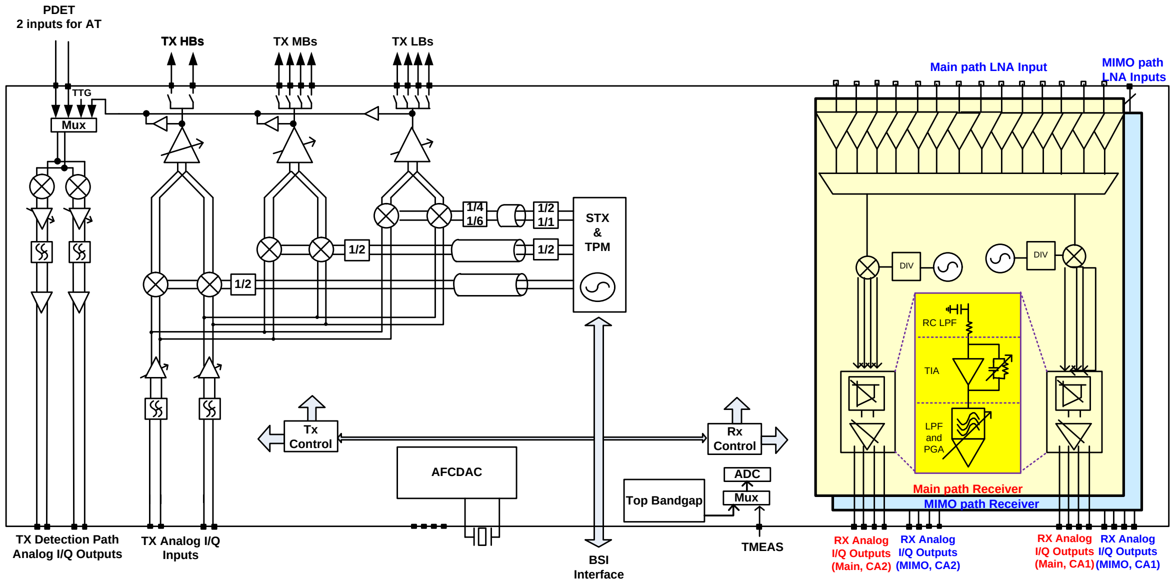
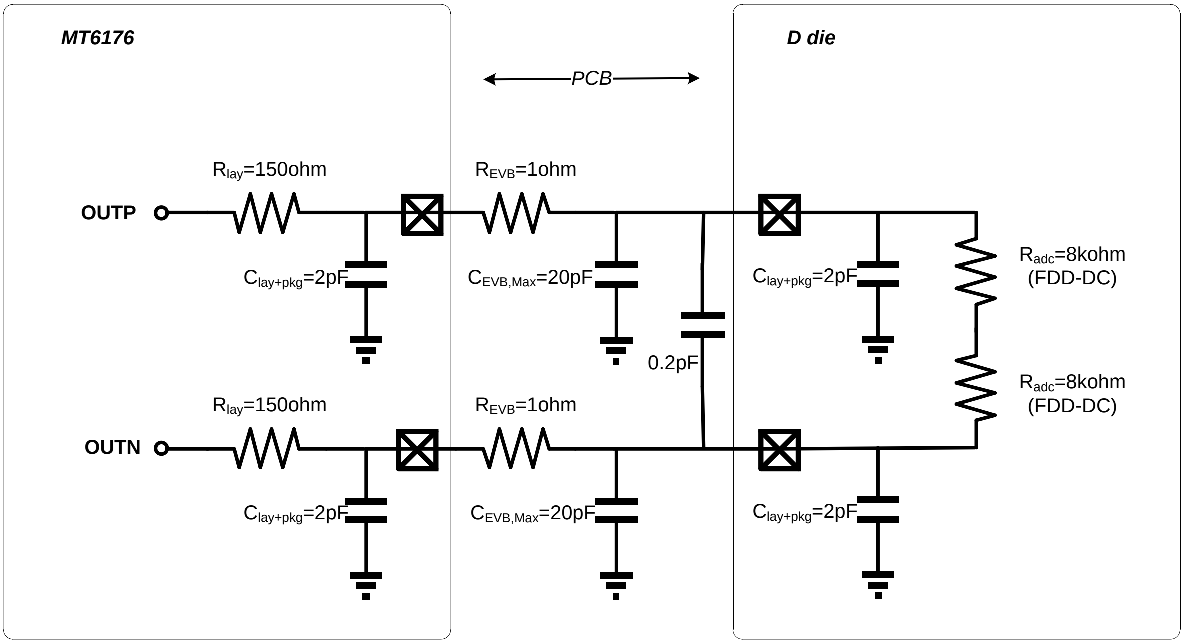


Figure 2-1. RFSYS block diagram

- RXIF IQ output loading model



For the applications whose bandwidth are beyond LTE20MHz, for example NC-CA (LTE20M + LTE20M), we highly recommend PCB loading should be small enough (<13pF) to avoid extra drooping in band-edge and performance degradation. In our design, maximum PCB loading 20pF is

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allowed. You can achieve good performance as long as PCB loading is smaller than 20pF. Inevitably, in some special case the PCB IQ traces may be longer and make PCB loading larger, the value would be up to several tens of pF. In these cases, they will work well with function but performance will be degraded.

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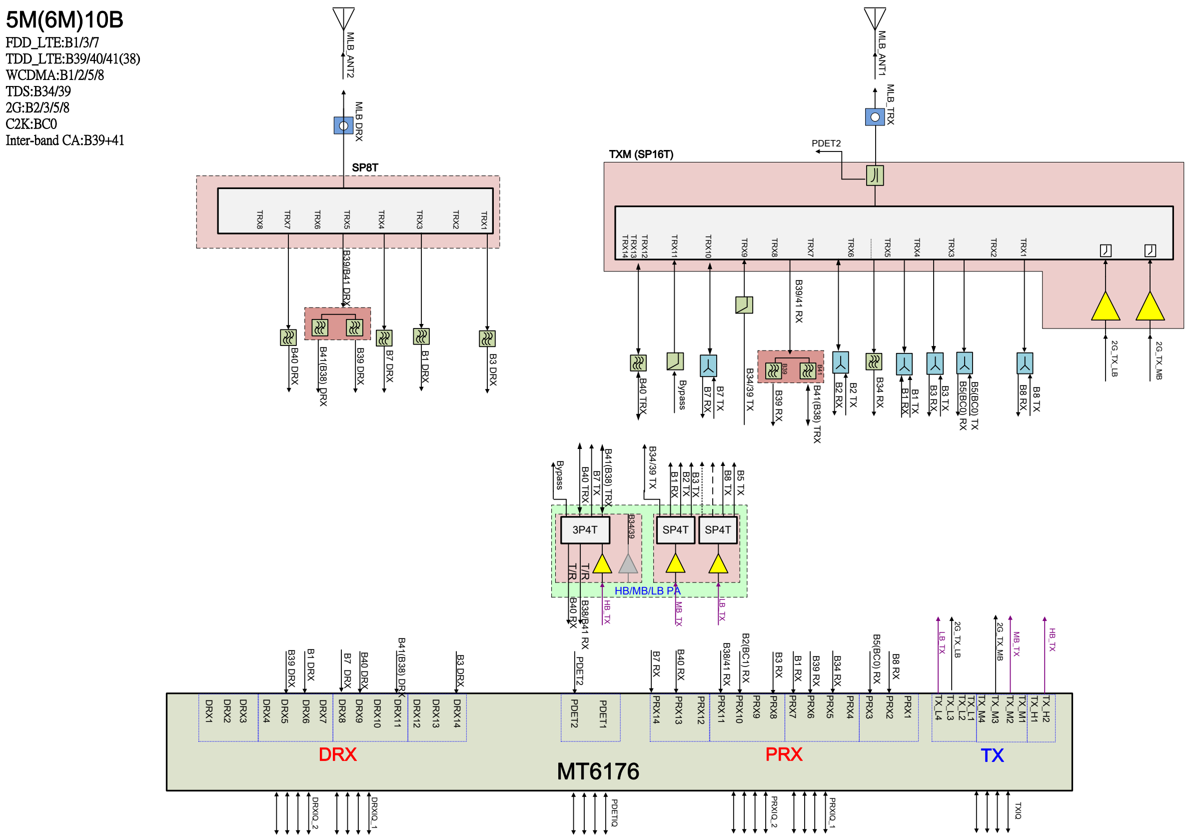

Figure 2-2. Applications diagram: example for 5M12B

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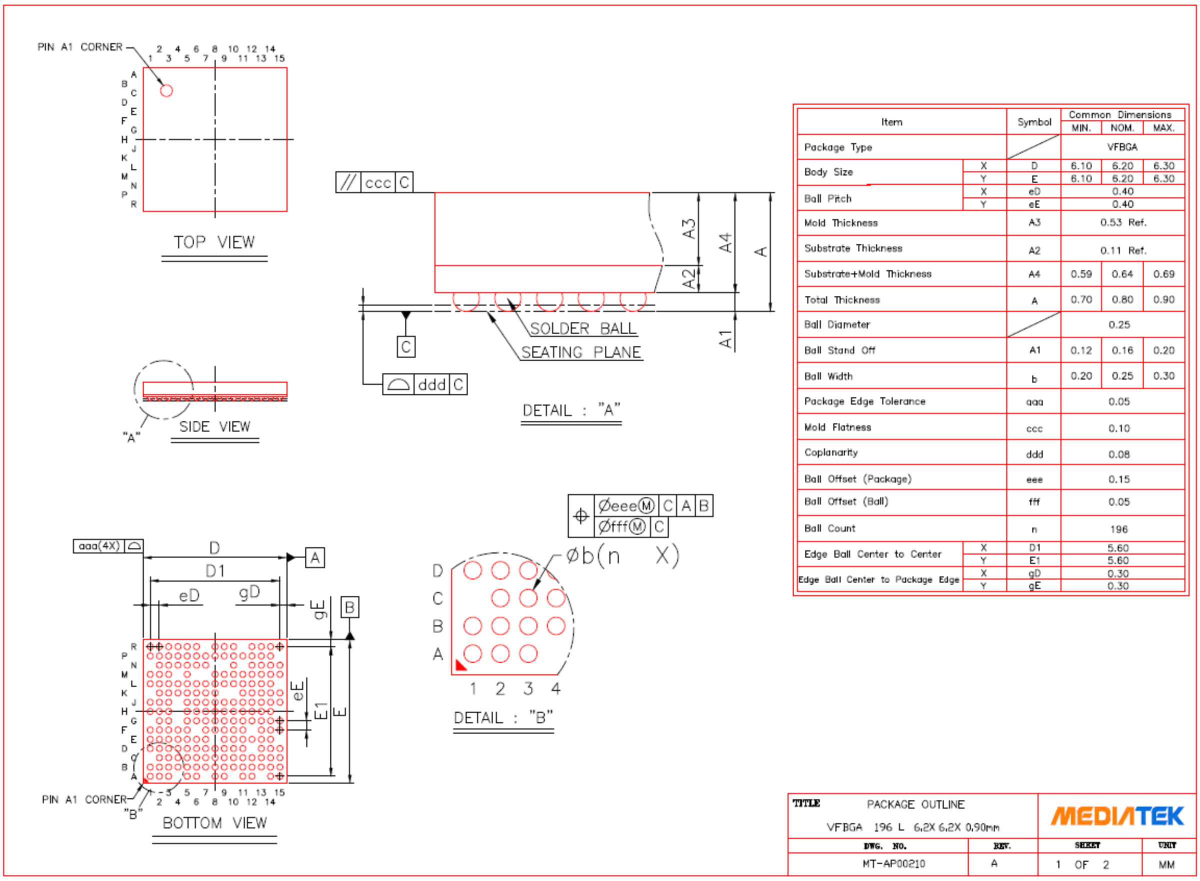
3 General Specifications

3.1 Packaging

Wirebond aS3 is currently considered for this product.

Parameter	Single die
Body Size (width/length/height)	6.2x6.2x0.9mm
Ball Spacing	0.4mm
Ball number	15x15



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type				VFBGA	
Body Size	X	D	6.10	6.20	6.30
	Y	E	6.10	6.20	6.30
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.53 Ref.	
Substrate Thickness		A2		0.11 Ref.	
Substrate+Mold Thickness		A4	0.59	0.64	0.69
Total Thickness		A	0.70	0.80	0.90
Ball Diameter				0.25	
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		196	
Edge Ball Center to Center	X	D1		5.60	
	Y	E1		5.60	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

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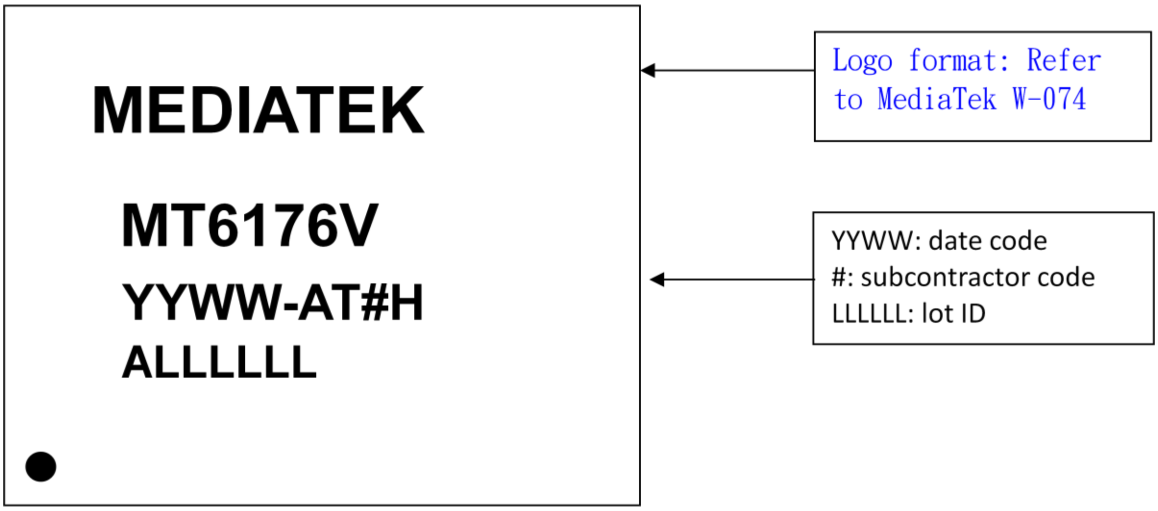
3.2 IC Marking



3.3 RF I/O List

Category	Pin Name				Description
	Name	Default	I/O	GPIO/RF pin	
RF I/O	PRX1		I	RF	Primary RX input 1
	PRX2		I	RF	Primary RX input 2
	PRX3		I	RF	Primary RX input 3
	PRX4		I	RF	Primary RX input 4
	PRX5		I	RF	Primary RX input 5
	PRX6		I	RF	Primary RX input 6
	PRX7		I	RF	Primary RX input 7
	PRX8		I	RF	Primary RX input 8
	PRX9		I	RF	Primary RX input 9
	PRX10		I	RF	Primary RX input 10
	PRX11		I	RF	Primary RX input 11
	PRX12		I	RF	Primary RX input 12
	PRX13		I	RF	Primary RX input 13
	PRX14		I	RF	Primary RX input 14
	DRX1		I	RF	Diversity RX input 1
	DRX2		I	RF	Diversity RX input 2
	DRX3		I	RF	Diversity RX input 3
	DRX4		I	RF	Diversity RX input 4
	DRX5		I	RF	Diversity RX input 5
	DRX6		I	RF	Diversity RX input 6
	DRX7		I	RF	Diversity RX input 7
	DRX8		I	RF	Diversity RX input 8
	DRX9		I	RF	Diversity RX input 9
	DRX10		I	RF	Diversity RX input 10
	DRX11		I	RF	Diversity RX input 11
	DRX12		I	RF	Diversity RX input 12
	DRX13		I	RF	Diversity RX input 13

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Category	Pin Name				Description
	Name	Default	I/O	GPIO/RF pin	
	DRX14		I	RF	Diversity RX input 14
	TX_HB1		O	RF	TX HB1 output
	TX_HB2		O	RF	TX HB2 output
	TX_MB1		O	RF	TX MB1 output
	TX_MB2		O	RF	TX MB2 output
	TX_MB3		O	RF	TX MB3 output
	TX_MB4		O	RF	TX MB4 output
	TX_LB1		O	RF	TX LB1 output
	TX_LB2		O	RF	TX LB2 output
	TX_LB3		O	RF	TX LB3 output
	TX_LB4		O	RF	TX LB4 output
	TXDET1		I	RF	TX detection path input 1
	TXDET2		I	RF	TX detection path input 2
BB I/O	PRX_BB1_IP		O	BB	RX1 BB I output
	PRX_BB1_IN		O	BB	RX1 BB I output
	PRX_BB1_QP		O	BB	RX1 BB Q output
	PRX_BB1_QN		O	BB	RX1 BB Q output
	PRX_BB2_IP		O	BB	RX2 BB I output
	PRX_BB2_IN		O	BB	RX2 BB I output
	PRX_BB2_QP		O	BB	RX2 BB Q output
	PRX_BB2_QN		O	BB	RX2 BB Q output
	PRX_BB1_IP		O	BB	RX1 diversity BB I output
	PRX_BB1_IN		O	BB	RX1 diversity BB I output
	PRX_BB1_QP		O	BB	RX1 diversity BB Q output
	PRX_BB1_QN		O	BB	RX1 diversity BB Q output
	PRX_BB2_IP		O	BB	RX2 diversity BB I output
	PRX_BB2_IN		O	BB	RX2 diversity BB I output
	PRX_BB2_QP		O	BB	RX2 diversity BB Q output
	PRX_BB2_QN		O	BB	RX2 diversity BB Q output
	TX_BBIP		I	BB	TX BB I input
	TX_BBIN		I	BB	TX BB I input
	TX_BBQN		I	BB	TX BB Q input
	TX_BBQP		I	BB	TX BB Q input
	DET_BBIP		O	BB	TX detection path I output, test pin 0
	DET_BBIN		O	BB	TX detection path I output, test pin 1
	DET_BBQP		O	BB	TX detection path Q output, test pin 2
	DET_BBQN		O	BB	TX detection path Q output, test pin 3
BSI Interface	BSI_EN		I	GPIO	BSI enable
	BSI_CLK		I	GPIO	BSI clock
	BSI_D0		I/O	GPIO	BSI input/output data
	BSI_D1		I/O	GPIO	BSI input/output data
	BSI_D2		I/O	GPIO	BSI input/output data
TCVCXO/ DCXO	XTAL1		I	RF	26MHz input
	XTAL2/ AFCDAC		I/O	RF	AFCDAC output

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Category	Pin Name				Description
	Name	Default	I/O	GPIO/RF pin	
	XO1		O	RF	
	XO2		O	RF	
	XO3		O	RF	
	XO4		O	RF	
	OUT_32K		O	RF	
	CLK_SEL	0	I		
	EN_BB		I		Global static enable
	32K_EN	0	I		TCVCXO
	XMODE	0	I		TCVCXO
Test Ports	TMEAS		I	DC	Temperature measurement
	RCAL		O	DC	External resistor calibration pin
Voltage Supply	VDD_RXHF		VDD	RF	DCDC 1.8V supply for RX
	VDD_RXLF		VDD	RF	DCDC 1.8V supply for RX
	VDD_RXLV		VDD	RF	DCDC 1.1V supply for RX
	VDD_TXHF		VDD	RF	DCDC 1.8V supply for TX and STX
	VDD_TXLV		VDD	RF	DCDC 1.1V supply for TX
	VDD_SXLF		VDD	RF	DCDC 1.8V supply for STX
	VDD_SXLV		VDD	RF	DCDC 1.1V supply for STX
	VIO		VDD	RF	Always on 1.8V for digital
	VDCXO_DIG		VDD	RF	Always on 1.8V for digital
	VTCXO		VDD	RF	2.3V for DCXO/TCVCXO
	V23_ESD1		VDD	RF	2.3V for ESD power.
	TXO_GND		GND	RF	TX output ground
	GND		GND	RF	RF ground

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3.4 Ball Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	DRX5	DRX6	DRX8		DRX11	DRX13		PRX13	PRX11		PRX8	PRX6		PRX4	PRX2
B	DRX4	DRX3	DRX7	DRX9	DRX10	DRX12	DRX14	PRX14	PRX12	PRX10	PRX9	PRX7	PRX5	PRX3	PRX1
C		DRX2	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
D	DRX1	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		GND	DRX_BB1_IN	DRX_BB1_IP
E	GND	GND	GND	GND	GND	GND	VDD_RXLF		GND	GND	GND	V23_ESD1	GND	DRX_BB1_QN	
F	DRX_BB2_IP	DRX_BB2_IN	GND	GND	GND		VDD_RXHF	VDD_RXLV	GND	GND	GND		GND	DRX_BB1_QP	PRX_BB1_IP
G		DRX_BB2_QN	GND		BSI_D2	GND	GND	GND	GND	GND	GND	GND	GND	PRX_BB1_QN	PRX_BB1_IN
H	PRX_BB2_IP	DRX_BB2_QP	GND		BSI_D1	BSI_EN	GND	GND	GND	GND	GND	GND	GND	PRX_BB1_QP	
J	PRX_BB2_IN	PRX_BB2_QN	GND		BSI_D0	BSI_CK	GND	GND	GND	GND	GND	GND	GND	TXO_GND	TXO_GND
K		PRX_BB2_QP	GND	GND	GND	GND	GND	GND			GND	GND	TXO_GND	TX_HB1	TX_HB2
L	EN_BB	GND	GND	GND	GND	DET_BBIP	DET_BBIN	DET_BBQP	DET_BBQN	GND	GND	GND	TXO_GND	TX_MB1	
M	CLK_SEL	VIO	VDCXO_DIG		GND			GND	VDD_SXLV	VDD_SXLF	GND	VDD_TXLV	TXO_GND	TX_MB3	TX_MB2
N		GND	GND	VTCXO	GND	GND	GND			VDD_TXHF		GND	TXO_GND	TX_LB1	TX_MB4
P	XO4	XO2	GND	GND	GND	XMODE	TMEAS	RCAL	GND	TX_BBQN	TX_BBQP	TX_BBIN	TXO_GND	TX_LB2	
R	XO1	XO3	OUT_32K	XTAL2	XTAL1	32K_EN		TXDET2	GND	TXDET1		TX_BBIP	TXO_GND	TX_LB4	TX_LB3

Figure 3-1. Ball map

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3.5 Absolute Maximum Ratings

Parameter	Conditions	Min.	Max.	Unit	Notes
Supply VTCXO23		-0.3	2.8	V	
Supply VIO18		-0.3	2.0	V	
Supply VXODIG		[-]	[-]	V	1. Connects to VIO18 in normal case 2. In ATPG mode, it connects to an independent supply with 1.3-V maximum voltage
Supply VRF18		-0.3	2.0	V	
Supply VRF11		-0.3	1.3	V	
Junction Temperature			125	°C	
ESD Protection	HBM – analog and digital I/O	±2000		V	
	HBM – RF I/O	±2000		V	PDET, Rx inputs, Tx outputs
	FICDM – analog and digital I/O	±250		V	target - no current corporate requirement
	FICDM– RF I/O	±250		V	PDET, Rx inputs, Tx outputs target - no current corporate requirement
	MM – analog and digital I/O	±200		V	
	MM – RF I/O	±100		V	PDET, Rx inputs, Tx outputs

Notes

1. No DC input should be directly applied to the Rx inputs.
2. Tx output: No DC should be applied under any circumstances (AC coupling required for those PA's with DC at the input).

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3.6 Operating Conditions

Within the operating range the IC operates as per the functional description.

Parameter	Conditions	Min.	Nom.	Max.	Unit
Supply VIO18		1.7	1.8	2	V
Supply VRF18		1.75	1.81	2	V
Supply VRF11		1.11	1.2	1.3	V
Linear Supply VTCXO23		2.3	2.375	2.45	V
Supply VXODIG	Normal function mode	Connects to VIO18			
Supply VXODIG	ATPG mode – LDO's bypassed in this mode	1.1	1.2	1.3	V
Receiver Front End					
RX input frequency range	See Receiver Section for detailed frequency ranges				
Transmitter					
Tx Frequency Range	See Transmitter Section for detailed frequency ranges				
Tx O/P VSWR	All Phases ZL = 50Ω			2:1	
Reference Clock Input (VCTCXO)					
Reference Clock Frequency			26.0		MHz
Reference Clock Input Voltage Swing	AC coupled at input pin	700		1500	mVpp
Duty Cycle		40		60	%
Phase Noise – note 2	@ F_{offset} = 100Hz		<-103	-100	dBc/Hz
	@ F_{offset} = 1KHz		<-133	-130	dBc/Hz
	@ F_{offset} = 10KHz		<-147	-144	dBc/Hz
	@ F_{offset} = 100KHz		<-149	-146	dBc/Hz
Harmonic Content	HD2 @ 52MHz			-8	dBc
	HD3 @ 78MHz			-10	dBc
	HD4 @ 104MHz			-20	dBc
Start-up time	|Δf|<1ppm to >90% of final amplitude			3	ms

Note 1

The supportable ambient temperature range will depend on the thermal impedance of the package used and the exact operational state as well as the end application thermal design (housing, PCB, etc).

Operation/Test condition	PCB temperature (°C)
TTC	+25°
ETC	-30° to +85°

Note 2

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The input clock requirement specified is defined to meet receiver and transmitter phase noise requirements e.g. IC EVM specification. Certain connectivity requirements may require better specifications than this. See clock buffer in section [7]. The clock source can either be an external VCTCXO/VCXO module or alternatively another transceiver clock buffer when considering multiple transceiver applications.

3.7 BSI Speed

PAD Name	Normal Mode	Normal mode direction	ATPG mode	ATPG mode direction
BSI_CLK	BSI_CLK	I (60MHz)	SCLK	I (100MHz)
BSI_EN	BSI_EN	I (60MHz)	SCAN_ENABLE	I (100MHz)
BSI_DATA0	BSI_DATA0	Bi-directional (60MHz)	SCAN_IN	I (100MHz)
BSI_DATA1	BSI_DATA1	Bi-directional (60MHz)	SCAN_OUT	O (100MHz)
BSI_DATA2	BSI_DATA2	Bi-directional (60MHz)	ATPG_RESETB	I (100MHz)

3.8 Deep Sleep Current

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Leakage Current						
VIO18 Leakage Current	I_{leak}		0.17	0.40	uA	1) VIO18 is on 2) ENBB is off 3) VRF18/12 are off

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4 Supply Specification

4.1 External Power Supplies and Interfaces

The RFSYS macro operates from four power supplies.

Supply name	Usage	Regulator type	Output voltage
VTCXO23	Regulated supply for VCTCXO	Linear	2.375V
VRF18	LDO supply (from system DCDC) for all major sub- systems	Linear with ripple	1.81V
VRF11	LDO supply (from system DCDC) for all major sub- systems	Linear with ripple	1.2V
VIO18	LDO supply (from system DCDC) ; Always-on supply for interface and register retention	Linear with ripple	1.8V
VXODIG	Connects to VIO18 in normal mode	Linear or Switching	1.8V

4.2 Power Requirements

Take PMIC MT6351 as reference:

IP name	Input source	VOUT(V) range /option	Voltage accuracy/feature support
VTCXO23	VBAT: 3.0V ~ 4.8V	2.375	AC+DC=+/-3%(DC trimming) @current profile(TBD)
VRF18 (from VS1)	P: VS1 2.0 +/-5% Full Performance: VS1≧Vout+150mV C: VBAT: 3.0V ~ 4.8V	1.81	DC:+/-50mV AC: +/-35mV, (settle 10us) @current profile 1. 25-> 350mA@80mA/us 2. freq ≦500kHz(pulse interval=10us~1ms) 3. general transient spec 4. detail spec refer LDO test case 5. PSRR=20dB: 217Hz ~3MHz 6. DC Vrange:2.0~1.78 7. AC Vrange:2.0~(1.78-35mV AC), (10us recover to 1.78V)
VRF12 (from VS2)	P: VS2 1.35 +/-5% Full Performance: VS2≧Vout+150mV C: VBAT: 3.0V ~ 4.8V	1.20	DC Vrange: +/-70mV AC: +/-20mV, (settle time 10us) @current profile 1. 10mA-> 105mA@0.2us 2. freq ≦500kHz(pulse interval=10us~1ms) 3. general transient spec 4. detail spec refer LDO test case 5.PSRR= 5dB: 217Hz ~3MHz 6. DC Vrange: 1.3~1.15 7. AC Vrange: 1.3~(1.15-20mV AC), (10us recover to 1.15)

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IP name	Input source	VOUT(V) range /option	Voltage accuracy/feature support
VIO18 (from VS1)	P: VS1 2.0 +/- 5% Full Performance: VS1≧Vout+150mV C: VBAT: 3.0V ~ 4.8V	1.8	DC+AC: +/- 100mV @current profile 1. 1-> 50mA/@50mA/us(emmc5.0) 2. 50->400mA@175mA/us(emmc5.0) 3. general transient spec Power on sequence for DRAM need special consideration
VS1	VBAT; 2.6V ~ 4.8V	1.9V ~ 2.2V, (50mV/step)	DC (PWM)+AC+Ripple ≦+/-5% PFM DC: -1 % ~ +3.5 % Mode transition included in AC part.
VS2	VBAT; 2.6V ~ 4.8V	1.3V ~ 1.5V (50mV/step)	DC (PWM)+AC+Ripple ≦+/-5% PFM DC: -1 % ~ +3.5 % Mode transition included in AC part.

4.3 Power Domains

The circuit block power diagram is shown below:

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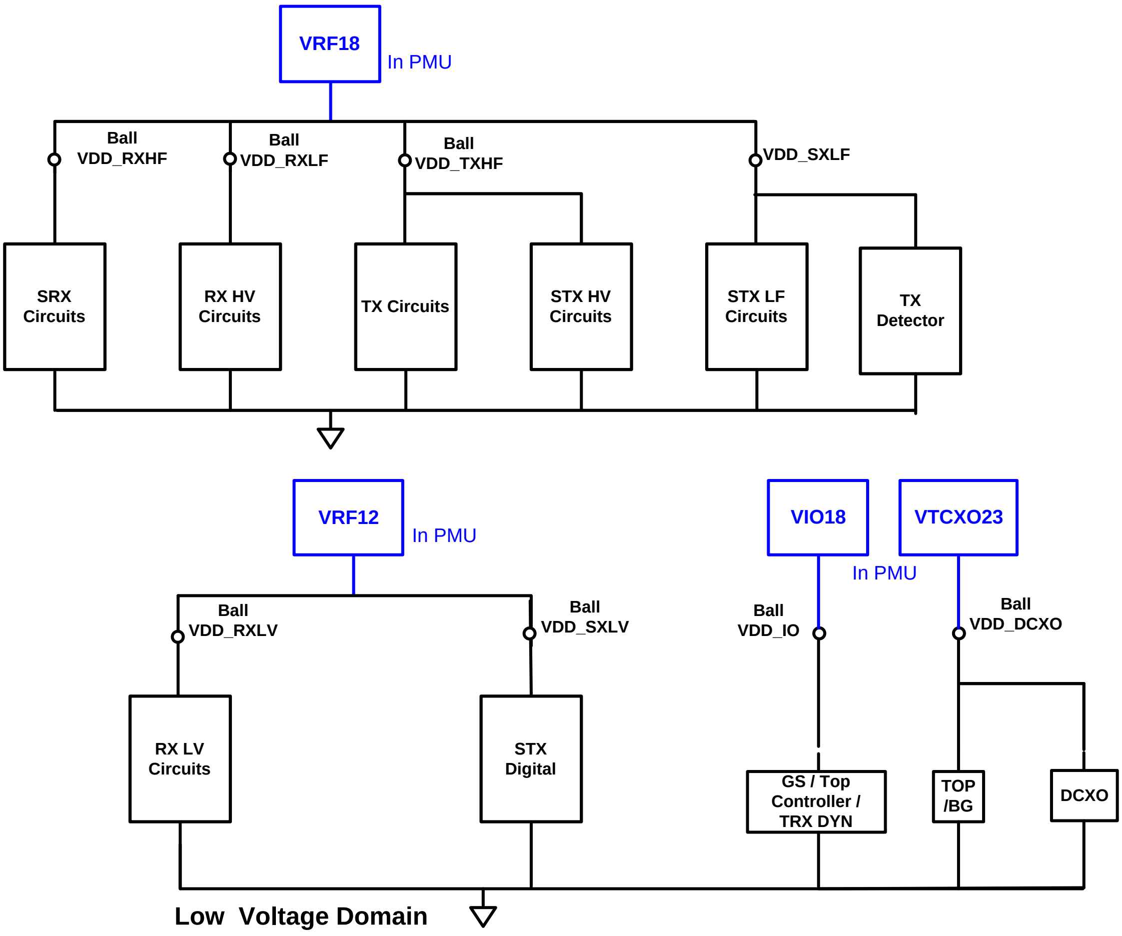

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5 Reference Clock Specification

MT6176 RF system integrates an AFCDAC for external VCTCXO. XTAL1 is the VCTCXO clock input pin and XTAL2 pin is the AFCDAC output.

5.1 Reference Input Buffer Specification (XTAL1/REFIN)

Parameter	Conditions	Min.	Nom.	Max.	Unit
Input Impedance – Rp	Rp || Cp @ 26MHz	3	10		kΩ
Input Impedance – Cp	Rp || Cp @ 26MHz		10	12	pF

The XTAL1 pin DC level should be 0~2.4V.

5.2 AFCDAC

Includes voltage reference generator

Parameter	Description / Condition	Min.	Typ.	Max.	Unit
FS – sampling rate	Event driven DAC => updated when new value written via BSI to DCXO_DIGITAL - Typically update rate is much slower			1.0833	MSPS
Resolution			13		bit
Settling time	Full code jump, and 99% settling after RC filter			1000	µsec
	70 code jump, and 99% settling after RC filter			166	µsec
	6 code jump, and 99% settling after RC filter			48	µsec
Power down glitch	The overshoot while power down (after output cap 1nF)			10	mV
Full Scale Range	Maximum Output Voltage (0x3FF)	2.0			V
	Minimum Output Voltage (0x000)			0.3	V
	Range (GAINSEL=0) – centered on nominal 1.15V		1.15		V
Cp	Load Capacitance		1	10	nF
PSRR	All conditions DC-100KHz	43			dB
DNL	Code 0 ~ 8191, after RC filter, output voltage 0.35~2.45V (GAINSEL= 0)	-1		+1	LSB
INL	Code 0 ~ 8191, after RC filter, output voltage 0.35~2.45V (GAINSEL = 0)	-32		+32	LSB
AVDD	Analog Power Supply	2.3	2.375	2.45	V
Supply current	Power-up		500		µA
	Power-Down, 85degC			1	µA

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5.3 26MHz Clock Output Buffer(s) Specification

There are at most four 26MHz clock output buffers (XO1/XO2/XO3/XO4). They can provide 26MHz clock to other chips.

Parameter	Description / Condition	Min.	Typ.	Max.	Unit
Buffer output Swing	Square wave @ Zload= Rp || Cp	700		1200	mVp-p
Zload (Rp||Cp)	Rp	3			kΩ
	Cp			30	pF
Duty Cycle		40		60	%
Rise / Fall Time	20% to 80% of signal swing @ Cload=30pF [normal drive mode]			6.5	ns
SSB phase noise	1Hz offset [30pF load, normal drive mode]			-50	dBc/Hz
	5Hz offset [30pF load, normal drive mode]			-73	dBc/Hz
	10Hz offset [30pF load, normal drive mode]			-80	dBc/Hz
	100Hz offset [30pF load, normal drive mode]			-105	dBc/Hz
	1kHz offset [30pF load, normal drive mode]			-131	dBc/Hz
	10kHz offset [30pF load, normal drive mode]			-144	dBc/Hz
	100KHz offset [30pF load, normal drive mode]			-150	dBc/Hz
Current Consumption	Cload = 20pF (each buffer)		1.0		mA

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6 Transmitter

All transmitter characteristics are listed in this section. Typical specifications are for mid-band channel frequency, and under typical operating conditions. Min/Max specifications are for extreme operating voltage and temperature conditions.

6.1 Tx Block Diagram

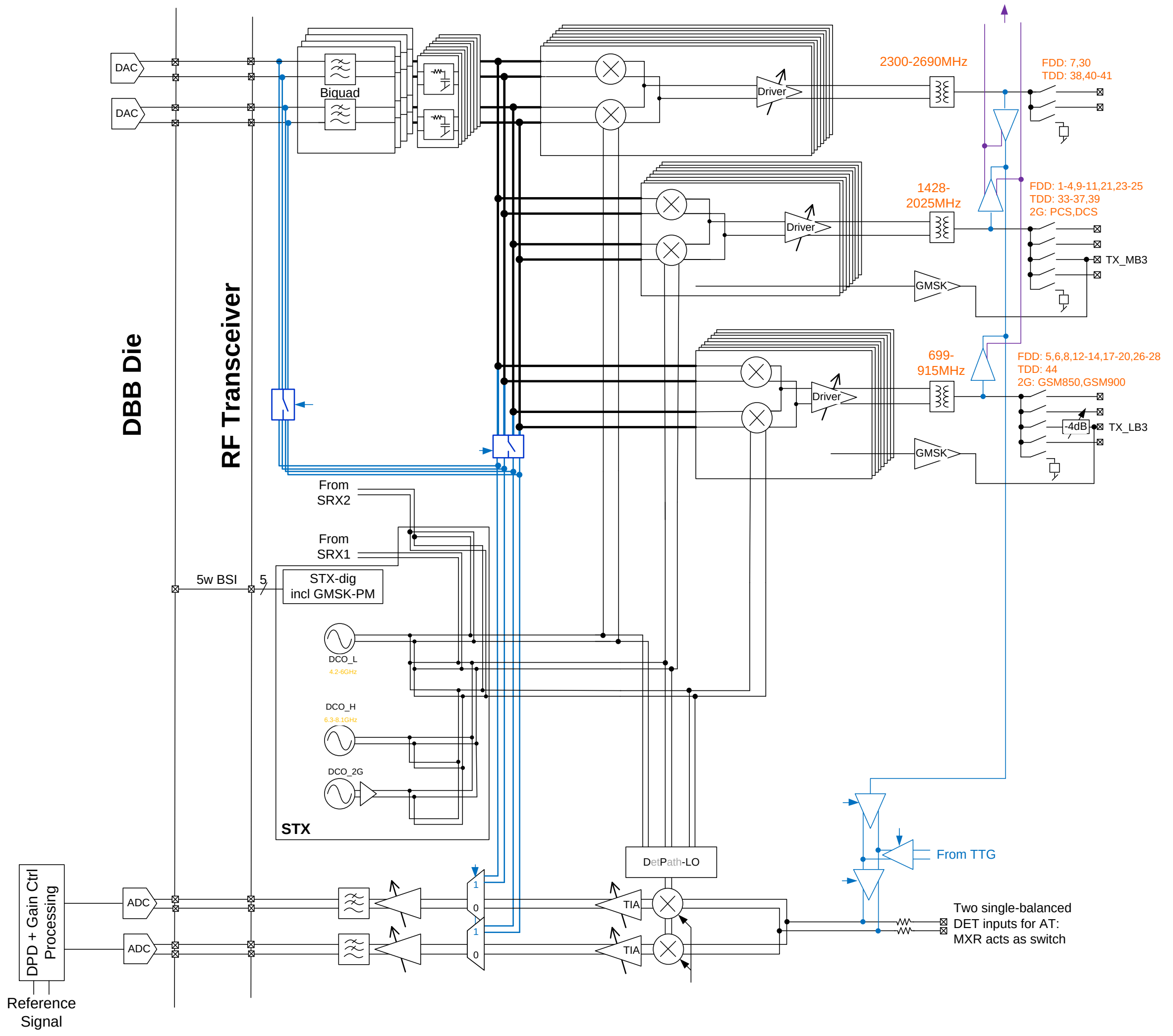

Figure 6-1. Tx block diagram

The transmitter is designed for high performance and low power consumption. It consists of three signal paths: low-band, mid-band and high-band (LB, MB, HB). The three paths share a common analog base-band active low-pass filter and a common passive RC low-pass filter. After that, the I/Q baseband signals are up-converted by one of three fully-differential passive mixers and amplified by

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the RF driver (PGA). The differential output is converted to single-ended using a balun. Finally the single-ended RF signal is routed to the desired output pin by the output switch. Note that only one TX-path and one output pin switch are active at a time. Singled-ended Tx signals at the output of the three signal paths (LB, MB, HB) are connected together to a common detector path used for calibration.

Each signal path (LB, MB, HB) has its corresponding LO distribution circuitry. The LO distribution design is optimized for low power consumption. The Detector path also has two RF inputs for high accuracy power control and Digital Predistortion (DPD).

6.2 4G FDD/TDD Transmitter Chain Performance Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
4G FDD/TDD Transmitter Output						
Output Return Loss	S_{22}		-6		dB	50 load
Output Power Band 1 Band 7 Band 8 Band 40	P_{max}		 -2.0 -0.6 -0.7 -0.6	 1.8 4.1 3.2 4.5	 dBm dBm dBm dBm	1) Pmax: ACLR<Spec 2) Pout (Typ): Pout with Typical front end components 3) Pout Can exceed Pmax in typical conditions
Min Output Power, all bands	P_{min}		-65		dBm	
RF Output Freq. Response HB LB	P		 1 1		 dB dB	
EUTRA ACLR (Full RB) Band 1 Band 7 Band 8 Band 40			 -46 -45 -45 -45		 dB dB dB dB	At Pout = Pmax
UTRA1 ACLR (Full RB) Band 1 Band 7 Band 8 Band 40			 -48 -48 -49 -45		 dB dB dB dB	At Pout = Pmax
EUTRA ACLR (Partial RB) Band 1 Band 7 Band 8 Band 40			 -42 -40 -43 -40		 dB dB dB dB	At Pout = Pmax(Min)
RMS EVM Band 1 Band 7 Band 8 Band 40			 2 2 2 2		 % % % %	Pout > -14dBm

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Noise in RX Band 1 Band 2 Band 7 Band 8 Band 13,14			 -162 -160 -160 -159 -156		 dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz	 At Pout = -2.0 dBm At Pout = 0.4 dBm At Pout = -0.6 dBm At Pout = -0.7 dBm At Pout = -2.2 dBm
Additional spurious emission (NS_07 for Flo-3Fbb) Band 13			-68		dBc	Pout = Pmax Spurious measurement RBW = 6.2KHz Peak search

6.3 4G FDD/TDD CCA (Cat7) Transmitter Chain Performance Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
4G FDD/TDD Transmitter Output						
Output Power (16QAM FRB) Band 1 Band 3 Band 7 Band 39 B38, B40, B41	P_{max}			 -1.2 0.5 1.1 1.0 1.5	 dBm dBm dBm dBm dBm	1) Pmax: ACLR<Spec 2) Pout (Typ): Pout with Typical front end components 3) Pout Can exceed Pmax in typical conditions
Min Output Power, all bands	P_{min}		-65		dBm	
RF Output Freq. Response	P		1		dB	
EUTRA ACLR (Full RB) Band 1 Band 3 Band 7 Band 39 B38, B40, B41			 -46 -47 -45 -46 -44		 dB dB dB dB	At Pout = Pmax
UTRA1 ACLR (Full RB) Band 1 Band 3 Band 7 Band 39 B38, B40, B41			 -51 -50 -50 -50 -49		 dB dB dB dB	At Pout = Pmax
RMS EVM (QPSK, 16QAM, 64QAM) Band 1 Band 3 Band 7 Band 39 B38, B40, B41			 2.5 2.5 2.5 2.5 2.5		 % % % %	Pout > -14dBm

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Noise in RX Band 1 Band 3 Band 7 Band 41			 -161 -156.5 -158 -163		 dBc/Hz dBc/Hz dBc/Hz dBc/Hz	 At Pout = 0 dBm At Pout = -0.3 dBm At Pout = -0 dBm At Pout = -0.4 dBm

6.4 3G FDD Transmitter Chain Performance Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
3G FDD Transmitter Output						
Output Return Loss	S_{22}		-6		dB	50 load
Max Output Power Band 1 Band 2 Band 5 Band 8	P_{max}			 3 3 2 2	dBm	R99 1) Pmax: ACLR<Spec 2) Pout Can exceed Pmax in typical conditions
Min Output Power	P_{min}		-72		dBm	With 4dB digital backoff
Max Output Power (R6 16QAM)	P_{max}		2		dBm	at B1
Min Output Power (R6 16QAM)	P_{min}		-76		dBm	With 4dB digital backoff
RF Output Frequency Response	P		0.5		dB	±2.5MHz offset
ACLR1 (R99) Band 1 Band 2 Band 5 Band 8			 -50 -50 -51 -51		dBc	 Pout=3 dBm Pout=3 dBm Pout=2 dBm Pout=2 dBm
ACLR2 (R99) Band 1 Band 2 Band 5 Band 8			 -65 -66 -67 -67		dBc	 Pout=3 dBm Pout=3 dBm Pout=2 dBm Pout=2 dBm
RMS EVM (R99) Band 1 Band 2 Band 5 Band 8			 2.7 2.6 2.5 2.4		%	 Pout=3 dBm Pout=3 dBm Pout=2 dBm Pout=2 dBm

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Peak EVM (R99)			8.6		%	Pout=5dBm
RMS EVM (R6 16QAM)			3		%	
Peak EVM (R6 16QAM)			11		%	
Noise Emissions						
Band I, noise in RX			-162		dBc/Hz	Pout= -2 dBm
Band II, noise in RX			-160		dBc/Hz	Pout= -0.4 dBm
Band V, noise in RX			-159		dBc/Hz	Pout= -2.05 dBm
Band VIII, noise in RX			-161		dBc/Hz	Pout= -0.65 dBm

6.5 3G TDD Transmitter Chain Performance Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
3G TDD Transmitter Output						
Output Return Loss	S_{22}		-6		dB	50 load
Max Output Power (QPSK)	P_{max}			4	dBm	at B40 1) Pmax: ACLR<Spec 2) Pout can exceed Pmax in typical conditions
Min Output Power (QPSK)	P_{min}		-61		dBm	at B40
Max Output Power (16QAM)	P_{max}		3.5		dBm	at B40
Min Output Power (16QAM)	P_{min}		-64		dBm	at B40
RF Output Frequency Response	P		0.2		dB	±2.5MHz offset
ACLR1 (QPSK)			-49		dB	at Pout=1dBm
ACLR2 (QPSK)			-65		dB	at Pout=1dBm
RMS EVM (QPSK)			2.0		%	at Pout=1dBm
ACLR1 (16QAM)			-49		dB	at Pout=1dBm
ACLR2 (16QAM)			-65		dB	at Pout=1dBm
RMS EVM (16QAM)			2.0		%	at Pout=1dBm

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6.6 3G C2K Transmitter Chain Performance Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
3G FDD Transmitter Output						
Output Return Loss	S_{22}		-6		dB	50 load
Max Output Power, LB BC0 (Band 5) BC10 (Band 26)	P_{max}	2.3 1.9			dBm dBm	1) Pmax: ACLR<Spec 2) Pout can exceed Pmax in typical conditions
Max Output Power, MB BC1 (Band 2) BC4 (Band 3) BC6 (Band 1) BC15 (Band 4)	P_{min}			2.9 2.8 1.0 2.1	dBm dBm dBm dBm	1) Pmax: ACLR<Spec 2) Pout can exceed Pmax in typical conditions
Min Output Power	P_{min}		-66		dBm	
RF Output Frequency Response	P		0.2		dB	±2.5MHz offset
SEM (1XRTT) at |Δf|:1.25~1.98MHz in 30kHz BW at |Δf|:1.98~4MHz in 30kHz BW			-59 -68	-62 -63	dBc dBc	
SEM (EVDO) at |Δf|:1.25~1.98MHz in 30kHz BW at |Δf|:1.98~4MHz in 30kHz BW			-56 -66	-51 -63	dBc dBc	
RMS EVM			2.7		%	
Peak EVM			8.6		%	
Carrier suppression				-40	dB	calibrated
Peak EVM (R6 16QAM)				-40	dB	calibrated
Noise Emissions						
BC6, noise in RX			-160		dBc/Hz	
BC1, noise in RX			-158		dBc/Hz	
BC0, noise in RX			-158		dBc/Hz	
BC10, noise in RX			-158		dBc/Hz	

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6.7 2G Transmitter Chain Performance Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
2G Transmitter Output						
Output Return Loss	S_{22}		-6		dB	50 load
Max Output Power, LB (GMSK)	P_{max}		3		dBm	
Max Output Power, HB (GMSK)	P_{max}		3		dBm	
Max Output Power, LB (8PSK)	P_{max}			1	dBm	1) Pmax: ORFS<Spec 2) Pout can exceed Pmax in typical conditions
Max Output Power, HB (8PSK)	P_{max}			1	dBm	1) Pmax: ORFS<Spec 2) Pout can exceed Pmax in typical conditions
Min Output Power (8PSK)	P_{min}		-40		dBm	
ORFS 400k, LB (GMSK)	$ORFS_{400k}$		-69		dBc	
ORFS 400k, HB (GMSK)	$ORFS_{400k}$		-66		dBc	
ORFS 400k, LB (8PSK)	$ORFS_{400k}$		-64		dBc	
ORFS 400k, HB (8PSK)	$ORFS_{400k}$		-65		dBc	
Modulation accuracy (GMSK)						
RMS phase error, LB	RMS		0.5		deg	
RMS phase error, HB	RMS		0.7		deg	
PEAK phase error, LB	Peak		1.9		deg	
PEAK phase error, HB	Peak		2.0		deg	
Modulation accuracy (8PSK)						
RMS EVM, LB	EVM_{RMS}		1.5		%	
RMS EVM, HB	EVM_{RMS}		2.0		%	
Peak EVM, LB	EVM_{Pk}		5		%	
Peak EVM, HB	EVM_{Pk}		6		%	
Origin offset	OOS		40		dB	
Noise Emissions (GMSK)						
20MHz offset, LB			-168		dBc/Hz	
32MHz offset, LB			-170		dBc/Hz	

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
20MHz offset, HB			-162		dBc/Hz	
32MHz offset, HB			-165		dBc/Hz	
Noise Emissions (8PSK)						
20MHz offset, LB			-159		dBc/Hz	Pout= -6dBm
32MHz offset, LB			-163		dBc/Hz	Pout= -6dBm
20MHz offset, HB			-160		dBc/Hz	Pout= -6dBm
32MHz offset, HB			-160		dBc/Hz	Pout= -6dBm

6.8 Transmitter Power Control Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Power Detector						
RF Input Frequency	F_{det}	699		2690	MHz	
Input Return Loss	S_{11}		-10		dB	Ref. impedance 50
Maximum Input Signal	$P_{det,max}$			0	dBm	
Minimum Input Signal	$P_{det,min}$	-40			dBm	
Measurement Accuracy					dB	
Measurement Time					us	

6.9 Harmonic Suppression

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
All Transmitter Outputs						
Harmonic Emissions						
2nd harmonic Band 1 Band 7 Band 5 Band 11 Band 13 Band 12 (Non HRM) Band 38			 -50 -51 -56 -56 -58 -57 -53		 dBc dBc dBc dBc dBc dBc dBc	

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
3rd harmonic Band 1 Band 7 Band 5 Band 11 Band 13 Band 12 (Non HRM) Band 38			 -20 -24 -19 -23 -54 -21 -23		 dBc dBc dBc dBc dBc dBc dBc	
4th harmonic Band 1 Band 7 Band 5 Band 11 Band 13 Band 12 (Non HRM) Band 38			 -53 -54 -63 -48 -64 -64 -54		 dBc dBc dBc dBc dBc dBc dBc	

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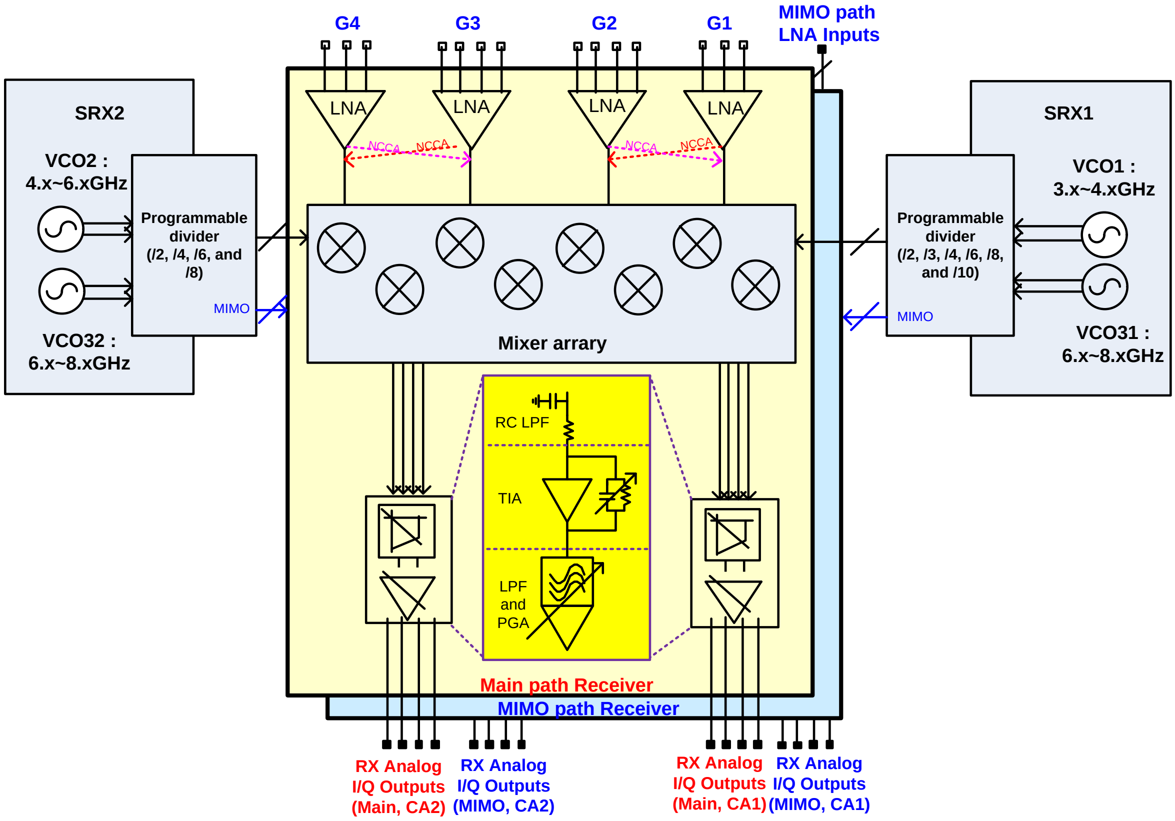
7 Receiver

The direct conversion/LIF receiver (RX) contains all active circuits for the complete receiver chain supporting LTE (TDD/FDD) with/without CA, single-cell (SC)/dual-cell (DC) 3G WCDMA, 3G TDSCDMA and 2G GSM/GPRS/EDGE (GGE) mode reception. The path contains a total of 14+14 single-ended input ports and 2+2 sets of I/Q outputs. 14 input ports are divided into four groups, G1 to G4, with shared LNA output. Each of these four group outputs could be down converted by two Rx synthesizers with maximum flexibility. Inter-band CA ports need to be assigned to different LNA groups, and intra-band non-contiguous CA signal could be down-converted by single path or two paths with different LO depending on the total bandwidth and power level difference.



The analog baseband filter is a low pass filter with programmable transfer function and gain controls. Besides, it contains an RC-calibration circuit, and a DC offset cancellation circuit (DCOC). The low-pass filter is configured as a 2nd-order Butterworth filter for LTE 1.4/3/5MHz BW, 3G FDD SC, 3G TDD, C2K and GGE modes. It is configured as a 3nd-order Butterworth filter for LTE 10/15/20MHz and 30/35/40M aggregated bandwidth for LTE-A DL CA. Receiver power ON/OFF sequence, LNA/band selection, total receiver gain including LNA, mixer and analog baseband and DCOC timing are controlled by digital circuits.

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In addition, IQ calibration is done by injecting an offset frequency test tone generated by the test tone generator (TTG) into the RX mixer. Additional on-the-fly IQ imbalance tracking may be added in the DBB without changing the receiver design. The timing and control of this calibration scheme are also controlled by L1 software and digital circuitry.

Receiver IP2 calibration is done by digital added algorithm to get the optimal receiver parameters in either factory, power-on, or pre-burst. This allows the transceiver to go with low cost front-end components.

The detailed receiver performance is summarized as followings.

7.1 TDSCDMA Specification

Parameter	Conditions	Min.	Nom.	Max.	Unit
Single-ended Input Impedance			50		Ω
Single-ended Input Return Loss	Note 1		-10		dB
Input Frequency	For all bands	1880		2400	MHz
Voltage Gain	Max gain: LNA G6; TIA HG; Filter gain=15dB. Note 2		53.6		dB
	Min gain: LNA G1; TIA MG; Filter gain=0dB. Note 2		2.6		dB
LNA Gain Step	LNA High ←→ Mid gain; source VSWR < 1.2		12		dB
	LNA Mid ←→ Low gain; source VSWR < 1.2		18		dB
3 dB Cut-Off Frequency	SC mode. Note 3		1		MHz
Noise Figure	Notes 1, 4; max gain.		2.5	3.5	dB
Input IP3	±3.2MHz and ±6MHz offset. LNA G6, TIA HG, Filter gain=15dB, -38dBm per tone	-12.5	-9.5		dBm
Input IP2	WiFi, max gain; (exclude external devices)	50			dBm
	±4.8MHz and ±4.9MHz LNA G6, TIA HG, Filter gain=15dB, -38dBm per tone	30	35		dBm

7.2 GGE Specification

Parameter	Conditions	Min.	Nom.	Max.	Unit
Single-ended Input Impedance			50		Ω
Single-ended Input Return Loss	Note 1		-10		dB
Input Frequency	For all bands	869		1990	MHz

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Parameter	Conditions	Min.	Nom.	Max.	Unit
Voltage Gain	Max gain: LNA G6; TIA HG; Filter gain=15dB. Note 2		53.6		dB
	Min gain: LNA G1; TIA MG; Filter gain=0dB. Note 2		2.6		dB
LNA Gain Step	LNA High ←→ Mid gain; source VSWR < 1.2		12		dB
	LNA Mid ←→ Low gain; source VSWR < 1.2		18		dB
3 dB Cut-Off Frequency	Note 3		1		MHz
Noise Figure	Notes 1, 4; max gain; high band		2.5	3.5	dB
	Notes 1, 4; max gain; low band		2.5	3.5	dB
IIP3	±0.8MHz and ±1.6MHz offset; LNA G6, TIA MG, Filter gain=6dB, -42dBm per tone	-12.5	-9.5		dBm
IIP2	WiFi, max gain; (exclude external devices)	50			dBm
	±5.94MHz and ±6.06MHz offset; LNA G6, TIA MG, Filter gain=9dB, -27dBm per tone	30	35		dBm

7.3 CDMA Specification

Parameter	Conditions	Min	Nom	Max	Unit
Single-ended Input Impedance			50		Ω
Single-ended Input Return Loss	Note 1		-10		dB
Input Frequency	For all bands	851		2170	MHz
Max. Voltage Gain	LNA G6; TIA HG and LPF=15dB.		53.6		dB
Min. Voltage Gain	LNA G1; TIA HG and LPF=0dB.		8.6		dB
LNA Gain Step G6: max gain G1: min gain	LNA G6 ←→ G5		6		dB
	LNA G5 ←→ G4		6		dB
	LNA G4 ←→ G3		6		dB
	LNA G3 ←→ G2		6		dB
	LNA G2 ←→ G1		6		dB
TIA Gain Step	TIA HG ←→ MG		6		dB
	TIA MG ←→ LG		6		dB
LPF Gain Step	Range from 0dB to 15dB, 3dB per step		3		dB
3 dB Cut-Off Frequency (TIA with LPF)	Note 2		1		MHz
Test condition 1 (LNA=G6, TIA=HG, LPF=15dB) [Sen]					
Noise Figure Notes 1, 3;			2.5	3.5	dB

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Parameter	Conditions	Min	Nom	Max	Unit
IIP3	LNA=G6, TIA=HG, LPF=15dB		-7		dBm
IIP2	At TX offset		55		dBm
Voltage Gain	LNA G6; TIA HG and LPF=15dB.		53.6		dB
Test condition 2 (LNA=G5, TIA=HG, LPF=3dB) [ACS1]					
Noise Figure Notes 1, 3;			7		dB
IIP3	LNA=G5, TIA=HG, LPF=3dB		-5		dBm
Voltage Gain	LNA=G5, TIA=HG, LPF=3dB		35.6		dB
Test condition 3 (LNA=G6, TIA=HG, LPF=6dB) [STD]					
Noise Figure Notes 1, 3;			5		dB
IIP3	LNA=G6, TIA=MG, LPF=6dB		-7		dBm
Voltage Gain	LNA=G6, TIA=MG, LPF=6dB		38.6		dB

7.4 WCDMA Specification

Parameter	Conditions	Min.	Nom.	Max.	Unit
Single-ended Input Impedance			50		Ω
Single-ended Input Return Loss	Note 1		-10		dB
Input Frequency	For all bands	869		2170	MHz
Max. Voltage Gain	LNA G6; TIA HG and LPF=15dB.		53.6		dB
Min. Voltage Gain	LNA G1; TIA HG and LPF=0dB.		8.6		dB
LNA Gain Step G6: max gain G1: min gain	LNA G6 ←→ G4		12		dB
	LNA G4 ←→ G1		18		dB
TIA Gain Step	Fixed TIA at HG				
LPF Gain Step	Range from 0dB to 15dB, 3dB per step		3		dB
3 dB Cut-Off Frequency (TIA with LPF)	BW=5MHz mode. Note 2		3		MHz
Test condition 1 (LNA=G6, TIA=HG, LPF=15dB) [Sen]					
Noise Figure Notes 1, 3;			2.5	3.5	dB
IIP3	LNA=G6, TIA=HG, LPF=15dB		-7		dBm
IIP2	At TX offset		55		dBm
Voltage Gain	LNA G6; TIA HG and LPF=15dB.		53.6		dB
Test condition 2 (LNA=G5, TIA=HG, LPF=6dB) [ACS1]					

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Parameter	Conditions	Min.	Nom.	Max.	Unit
Noise Figure Notes 1, 3;			6		dB
IIP3	LNA=G5, TIA=HG, LPF=6dB		-7		dBm
Voltage Gain	LNA G5; TIA HG and LPF=6dB.		38.6		dB
Test condition 3 (LNA=G6, TIA=HG, LPF=6dB) [NBB]					
Noise Figure Notes 1, 3;			3		dB
IIP3	LNA=G4, TIA=HG, LPF=6dB		-9		dBm
Voltage Gain	LNA= -30dBS; mixer = -6.9dB, TIA gain=63.5dBohm and LPF=6dB.		44.6		dB
Test condition 4 (LNA=G1, TIA=HG, LPF=6dB) [ACS2]					
Noise Figure Notes 1, 3;			26.5		dB
IIP3	LNA=G1, TIA=HG, LPF=6dB		7		dBm
Voltage Gain	LNA=G1, TIA=HG, LPF=6dB		14.6		dB
Test condition 5 (LNA=G1, TIA=HG, LPF=0dB) [Maximum Input]					
Noise Figure Notes 1, 3;			35		dB
Voltage Gain	LNA=G1, TIA=HG, LPF=0dB		8.6		dB

7.5 LTE Specification

- Non/inter-band/intra-band contiguous CA scenario

Parameter	Conditions	Min.	Nom.	Max.	Unit
Single-ended Input Impedance			50		Ω
Single-ended Input Return Loss	Note 1		-10		dB
Input Frequency	For all bands	703		2690	MHz
Max. Voltage Gain	LNA= G6, TIA=HG and LPF=15dB.		53.6		dB
Min. Voltage Gain	LNA= G1, TIA =MG and LPF=0dB.		2.6		dB
LNA Gain Step G6: max gain G1: min gain	LNA G6 ←→ G5		6		dB
	LNA G5 ←→ G4		6		dB
	LNA G4 ←→ G3		6		dB
	LNA G3 ←→ G2		6		dB
	LNA G2 ←→ G1		6		dB
TIA Gain Step	TIA HG ←→ MG		6		dB
	TIA MG ←→ LG		6		dB

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Parameter	Conditions	Min.	Nom.	Max.	Unit
LPF Gain Step	Range from 0dB to 18dB, 3dB per step		3		dB
3 dB Cut-Off Frequency (TIA with LPF)	BW=1.4MHz mode. Note 2		1		MHz
	BW=3MHz mode. Note 2		3		MHz
	BW=5MHz mode. Note 2		3		MHz
	BW=10MHz mode. Note 2		5		MHz
	BW=15MHz mode. Note 2		7.5		MHz
	BW=20MHz mode. Note 2		10		MHz
	BW=30MHz mode. Note 2		15.7		MHz
	BW=40MHz mode. Note 2		20.8		MHz
Test condition 1-1 (LNA=G6, TIA=HG, LPF=15dB) [Sen]					
Noise Figure Notes 1, 3;	frequency < 2300MHz		2.5	3.5	dB
	frequency > 2300MHz		2.8	3.8	dB
IIP3	LNA=G6, TIA=HG, LPF=15dB		-7		dBm
IIP2	At TX offset		55		dBm
Voltage Gain	LNA=G6, TIA=HG, LPF=15dB		53.6		dB
Test condition 2 (LNA=G6, TIA=MG, LPF=6dB) [ACS1]					
Noise Figure Notes 1, 3;	frequency < 2300MHz		5		dB
	frequency > 2300MHz		5		dB
IIP3	LNA=G6, TIA=MG, LPF=6dB		-7		dBm
Voltage Gain	LNA=G6, TIA=MG, LPF=6dB		38.6		dB
Test condition 3 (LNA=G4, TIA=MG, LPF=9dB) [NBB]					
Noise Figure Notes 1, 3;	frequency < 2300MHz		8		dB
	frequency > 2300MHz		8		dB
IIP3	LNA=G4, TIA=MG, LPF=9dB		0		dBm
Voltage Gain	LNA=G4, TIA=MG, LPF=9dB		29.6		dB
Test condition 4 (LNA=G2, TIA=MG, LPF=6dB) [ACS2]					
Noise Figure Notes 1, 3;	frequency < 2300MHz		26.5		dB
	frequency > 2300MHz		26.5		dB
IIP3	LNA=G1, TIA=MG, LPF=6dB		7		dBm
Voltage Gain	LNA=G1, TIA=MG, LPF=6dB		14.6		dB
Test condition 5 (LNA=G1, TIA=MG, LPF=0dB) [Maximum Input]					
Noise Figure Notes 1, 3;	frequency < 2300MHz		35		dB
	frequency > 2300MHz		35		dB
Voltage Gain	LNA=G1, TIA=MG, LPF=0dB		2.6		dB

Note 1: Source/Reference impedance: 50 Ω
Note 2: After RC calibration

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Note 3: No blockers.
Note 4: Includes RX LDO, LNA/MXR, SRX and LO path, TIA, and RXABB

- Intra-band non-contiguous CA scenario

Parameter	Conditions	Min.	Nom.	Max.	Unit
Single-ended Input Impedance			50		Ω
Single-ended Input Return Loss	Note 1		-10		dB
Input Frequency	For all bands	703		2690	MHz
Max. Voltage Gain	LNA= G6, TIA=HG and LPF=15dB.		53.6		dB
Min. Voltage Gain	LNA= G1, TIA =MG and LPF=0dB.		2.6		dB
LNA Gain Step G6: max gain G1: min gain	LNA G6 ←→ G5		6		dB
	LNA G5 ←→ G4		6		dB
	LNA G4 ←→ G3		6		dB
	LNA G3 ←→ G2		6		dB
	LNA G2 ←→ G1		6		dB
TIA Gain Step	TIA HG ←→ MG		6		dB
	TIA MG ←→ LG		6		dB
LPF Gain Step	Range from 0dB to 18dB, 3dB per step		3		dB
3 dB Cut-Off Frequency (TIA with LPF)	BW=1.4MHz mode. Note 2		1		MHz
	BW=3MHz mode. Note 2		3		MHz
	BW=5MHz mode. Note 2		3		MHz
	BW=10MHz mode. Note 2		5		MHz
	BW=15MHz mode. Note 2		7.5		MHz
	BW=20MHz mode. Note 2		10		MHz
	BW=30MHz mode. Note 2		15.7		MHz
	BW=40MHz mode. Note 2		20.8		MHz
Test condition 1-1 (LNA=G6, TIA=HG, LPF=15dB) [Sen]					
PCC Noise Figure Notes 1, 3;	frequency < 2300MHz		2.5	3.5	dB
	frequency > 2300MHz		2.8	3.8	dB
SCC Noise Figure Notes 1, 3;	frequency < 2300MHz		3	4	dB
	frequency > 2300MHz		3.3	4.3	dB
PCC IIP3	LNA=G6, TIA=HG, LPF=15dB		-7		dBm
SCC IIP3	LNA=G6, TIA=HG, LPF=15dB		-9		dBm
PCC IIP2	At TX offset		55		dBm
SCC IIP2 Note 5	TX offset > 50 MHz		55		dBm
	TX offset < 50 MHz		50		dBm

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Parameter	Conditions	Min.	Nom.	Max.	Unit
Voltage Gain	LNA=G6, TIA=HG, LPF=15dB		53.6		dB
Test condition 2 (LNA=G6, TIA=MG, LPF=6dB) [ACS1]					
PCC Noise Figure Notes 1, 3;	frequency < 2300MHz		5		dB
	frequency > 2300MHz		5		dB
SCC Noise Figure Notes 1, 3;	frequency < 2300MHz		6		dB
	frequency > 2300MHz		6		dB
PCC IIP3	LNA=G6, TIA=MG, LPF=6dB		-7		dBm
SCC IIP3	LNA=G6, TIA=MG, LPF=6dB		-9		dBm
Voltage Gain	LNA=G6, TIA=MG, LPF=6dB		38.6		dB
Test condition 3 (LNA=G4, TIA=MG, LPF=9dB) [NBB]					
PCC Noise Figure Notes 1, 3;	frequency < 2300MHz		8		dB
	frequency > 2300MHz		8		dB
SCC Noise Figure Notes 1, 3;	frequency < 2300MHz		10		dB
	frequency > 2300MHz		10		dB
PCC IIP3	LNA=G4, TIA=MG, LPF=9dB		0		dBm
SCC IIP3	LNA=G4, TIA=MG, LPF=9dB		-2		dBm
Voltage Gain	LNA=G4, TIA=MG, LPF=9dB		29.6		dB
Test condition 4 (LNA=G2, TIA=MG, LPF=6dB) [ACS2]					
PCC Noise Figure Notes 1, 3;	frequency < 2300MHz		26.5		dB
	frequency > 2300MHz		26.5		dB
PCC Noise Figure Notes 1, 3;	frequency < 2300MHz		26.5		dB
	frequency > 2300MHz		26.5		dB
PCC IIP3	LNA=G2, TIA=MG, LPF=6dB		7		dBm
SCC IIP3	LNA=G2, TIA=MG, LPF=6dB		5		dBm
Voltage Gain	LNA=G2, TIA=MG, LPF=6dB		14.6		dB
Test condition 5 (LNA=G1, TIA=MG, LPF=0dB) [Maximum Input]					
PCC Noise Figure Notes 1, 3;	frequency < 2300MHz		35		dB
	frequency > 2300MHz		35		dB
PCC Noise Figure Notes 1, 3;	frequency < 2300MHz		35		dB
	frequency > 2300MHz		35		dB
Voltage Gain	LNA=G1, TIA=MG, LPF=0dB		2.6		dB

Note 1: Source/Reference impedance: 50 Ω
Note 2: After RC calibration
Note 3: No blockers.
Note 4: Includes RX LDO, LNA/MXR, SRX and LO path, TIA, and RXABB
Note 5: For B7, SCC TX-offset IIP2 becomes 40 dBm

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8 Digital Control Interfaces

8.1 Introduction

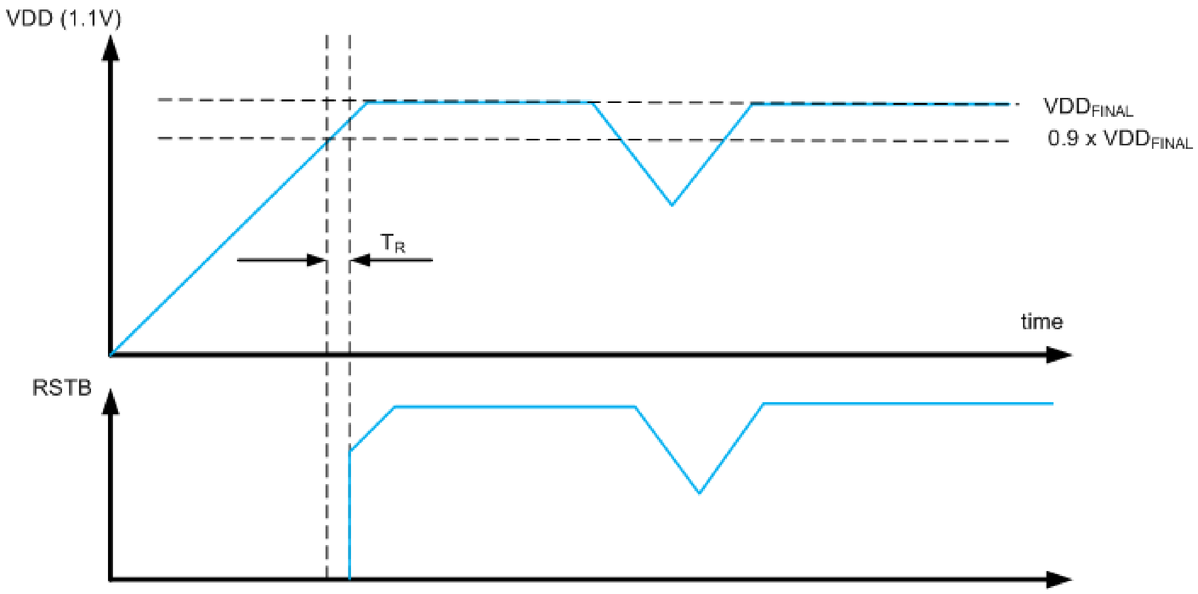
RFSYS is programmed through 5 BSI GPIO PADs. Both write and read operations are supported and 5 wires are used (3 bi-direction data pins, one clock pin, and one enable pin). All BSI interfaces are through VIO18 domain.

8.2 Power-on Reset

The chip includes two Power-On Reset (POR) operating from the static domain LDO's on the VXODIG domain. These operate on the DCXO_DIGITAL and GLOBAL_STATIC digital blocks from the 1.1V supply domain directly derived from VXODIG via LDO's. The designs are identical and since VXODIG is an "always-on" supply then a simplified implementation can be used - specifically there should not be situation where the VXODIG supply can drop after the internal LDO is enabled. The important point then is that the reset needs to be active for sufficiently long that the power supply has stabilized but short enough that the domain is available for BSI programming when requested.

In the case of the DCXO POR the LDO is directly enabled from the VXODIG supply. In the case of the GS LDO VXODIG is always present (in normal mode) and the LDO for this domain is enabled from the baseband.

The operation is shown in the figure below.



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Parameter	Conditions	Min	Nom	Max	Unit	Notes
Reset Active Time T_R	Over range of full VIO18 ramp times	5		200	µs	
VDD		0.8	1.1	1.25	V	
Trigger Point V_{TH}			0.9 x VDD		V	
Idd Quiescent current				<100	nA	

8.3 BSI Interface

The BSI Clock is designed to operate at a maximum frequency of 61.44 MHz, switching down to 30.72 MHz during the read back phase of a read operation.

The BSI clock has nominally a 50% duty cycle (< 40:60 should be guaranteed by the baseband clock generator). Following figure shows the timing diagram of write and read operations via BSI interface.

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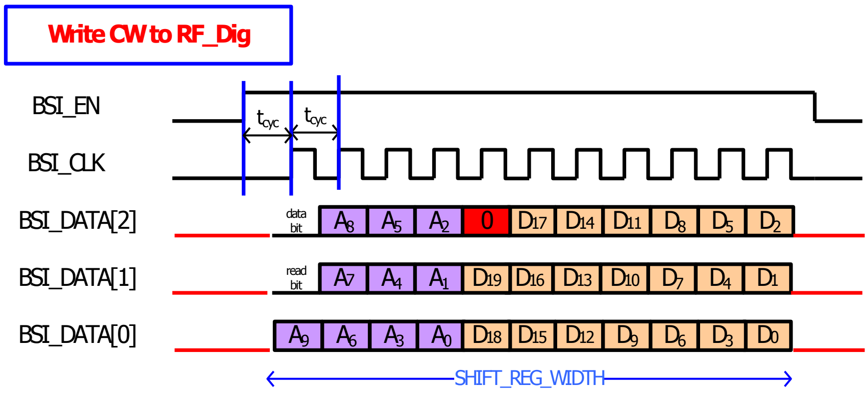

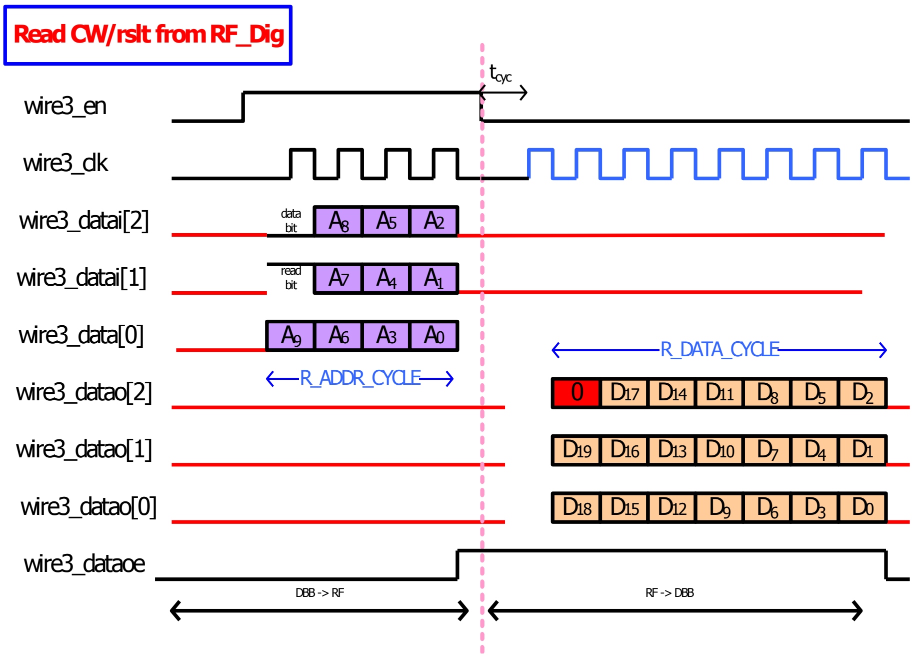

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